CLAIMS

What is claimed is:

1. A method of memory management, comprising:

providing multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

providing a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

establishing a bank queue for each bank in each channel for designating bank availability;

sending read or write requests to the tree memory controller;

checking, at the tree memory controller, the availability of each bank in a channel;

identifying a first available bank; and

executing the read request from the first available bank.

2. The method of claim 1 wherein the step of executing for a write access includes:

blocking all read requests;

confirming that data to be written is complete for the selected memory word length;

waiting for each bank queue to indicate bank availability for all banks;

initiating burst mode transfer of the completed data word to all banks concurrently.

3. The method of claim 1 wherein the memory devices comprise dynamic random access memory (DRAM) devices.

4. The method of claim 1 wherein the memory devices comprise fast cycle random access memory (FCRAM) devices.

5. The method of claim 1 wherein the banks of memory devices

are organized into two independent channels.

6. A method system, comprising:

multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

a bank queue for each bank in each channel for designating bank availability; and

means for sending read or write requests to the tree memory controller, said controller determining availability of a bank for reading data and executing the read request from a first available bank.

7. The system of claim 6 wherein the controller suspends all read requests during processing of a write request.

8. The system of claim 7 wherein the controller writes to all memory banks concurrently.

9. The system of claim 8 wherein all memory banks contain identical data.

10. The system of claim 6 wherein the memory banks comprise dynamic random access memory devices.

11. The system of claim 6 wherein the memory banks comprise fast cycle random access memory devices.

12. The system of claim 6 wherein the banks of memory devices are arranged in two independent channels.

13. The system of claim 6 wherein the minimum number of memory banks is determined by the ratio of the random cycle time to the random bank access delay.